Atty. Dkt. No 039153-5002 (G0166)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Xiang, Qi

Title: INTEGRATED CIRCUIT WITH TWO PHASE FUSE MATERIAL AND METHOD OF USING AND MAKING SAME

Appl. No.: 10/729,194

Filing Date: 12/5/2003

Examiner: Khem D. Nguyen

Art Unit: 2812

CERTIFICATE OF EXPRESS MAILING
I hereby certify that this correspondence is being deposited with the United States Postal Service's "Express Mail Post Office To Addressee" service under 37 C.F.R. § 1.10 on the date indicated below and is addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

(Express Mail Label Number) (Date of Deposit)

(Printed Name)

(Signature)

DECLARATION UNDER 37 C.F.R. § 1.131

Mail Stop AMENDMENT
Commissioner for Patents
PO Box 1450
Alexandria, Virginia 22313-1450

Sir:

I, Qi Xiang state and declare that:

1. I am the sole inventor of Claims 12-19 and 22-34 currently pending in U.S. Patent Application No. 10/729,194 entitled "INTEGRATED CIRCUIT WITH TWO PHASE FUSE MATERIAL AND METHOD OF USING AND MAKING SAME" (hereinafter "the '194 application").

2. I understand that in an Office Action dated June 22, 2005, Claims 12-19 and 22-34 were rejected as being unpatentable based in part on U.S. Patent No. 6,703,680 to Toyoshima., entitled "Programmable Element Programmed by Changes in Resistance Due to Phase Transition" (hereinafter "Toyoshima").

3. I understand based on the information provided on the front page of Toyoshima that Toyoshima was filed on December 31, 2001 as U.S. Patent Application No. 10/029,718.

4. At least by March 13, 2001, I conceived in the United States the ideas set forth in Claims 12-19 and 22-34 of the '194 application. Such conception is evidenced by the attached Exhibit A, which includes two invention disclosure forms pertaining to the subject matter of the present application dated March 13, 2001.

Atty. Dkt. No 039153-5002 (G0166)

5. Based on the conception of the ideas set forth in Claims 12-19 and 22-34 at least by March 13, 2001, the subject matter recited in Claims 12-19 and 22-34 was invented by me prior to the December 31, 2001 filing date of U.S. Patent Application No. 10/029,718.

6. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are true, and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the patent application or any patent issuing therefrom.

Date: 9/21/05 By: _____

Qi Xiang

AMD INVENTION DISCLOSURE

Legal Dept Ref# Gold

Sunnyvale x42110, return to MS 68

Rec'd date

Texas x55964 return to MS 562

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MAR 19 2001
AMD TECH. LAW DEPT.

AMD division / department: "B"

Technology to which the invention applies: HIP7/HIP8...(Bulk/SOI...)

AMD product or process to which invention applies (if any): K7/K8.....

Working title of invention: Poly NiSi Fuse Devices

Inventor's signature : _____ **date :** _____
Inventor's printed full name: Qi Xinag Citizenship: China
Employee #: 24395 Extension: 44771 Mail stop: 143 Home telephone:(408)517-0879
Dept #: 7360 Division name: STG Supervisor: Ming-Ren Lin Director Dave Kyser VP: Craig Sander
Residence address: 1119 Thames Drive, San Jose, CA 95129
Post Office address: Same as above

Co-Inventor's signature : _____ date :_____
Co-Inventor's printed full name: _____ Citizenship:_____
Employee #:_____ Extension:_____ Mail stop:_____ Home telephone:( )_____
Dept #:_____Division name:_____Supervisor:_____ Director_____VP:_____
Residence address:_____
Post Office address:_____

Co-Inventor's signature : _____ date :_____
Co-Inventor's printed full name: _____ Citizenship:_____
Employee #:_____ Extension:_____ Mail stop:_____ Home telephone:( )_____
Dept #:_____Division name:_____Supervisor:_____ Director_____VP:_____
Residence address:_____
Post Office address:_____

10/749,477

List on additional sheet if there are more Co-Inventors and list total number of inventors here:_____

Name of requested Patent Application preparation Attorney , if known, _____

Witness 1 initial: [illegible] Witness 2 initial: [illegible]

Exhibit A

AMD INVENTION DISCLOSURE Legal Dept ID#_____ Rec'd date_____
Sunnyvale x42110, return to MS 68, Texas x55964 return to MS 562

Identify known related art (patents, publications, products): Conventionally, people use EEPROM, Laser, oxide antifuse device and poly silicide (CoSi2/TiSi2) fuse device to form the discretionary connection function of a fuse device.

State the problem solved by this invention: This invention provide a small, nondestructive, process compatible and low voltage NiSi fuse device.

Brief description and/or sketch of invention (*please attach copies of AMD patent notebook pages, reports or drawings*):

In integrated circuits including CMOS ICs, it is often desirable to be able to permanently store information, or to form permanent connections on the circuits after it is manufactured. Fuse or devices forming fusible connection are frequently used for this purpose. Fuses can be used to program redundant elements to replace identical defective elements. Fuses can also be used to store die identification number or other information, or to adjust the speed of a circuit by adjusting the resistance of the signal path.

The conventional fuse devices, like EEPROM and oxide antifuse, need either thick oxide to sustain a charge on the floating node or much higher voltages than normal operating voltage supply, which are not viable for use on many of latest process technologies. Other conventional fuse devices, like the one is programmed using a laser to open link after the semiconductor device is processed and passivated, not only need extra processing step to blow and precise alignment to focus but also result in damages to the device and passivation layers.

Agglomeration of poly silicide has also been used to program fuse devices using CoSi2 and TiSi2. For the CoSi2 and TiSi2 poly fuse devices, a relatively high programming voltage is needed to generate enough heat and agglomerates the silicides.

This invention provides a small, nondestructive, process compatible and low voltage fuse device. As shown in Fig.1, a fusible link device is disposed on poly silicon that is on the top of a thick insulator films (SiO2 or SiN) on semiconductor substrate. The fusible link device of the invention has a fresh non-programmed resistance and includes a nickel mono-silicide (NiSi) layer on top of poly silicon layer. The NiSi layer is formed on the doped or undoped poly silicon layer. The electrical discontinuity is formed due to change of silicide phase from NiSi into high resistivity phase of nickel disilicide (NiSi2) when programming current is applied, such that the resistance of the fusible link device can be selectively increased to a higher programmed resistance. Because the NiSi layer has much lower sheet resistance than the NiSi2 layer, the resistance of the fuse device increases accordingly. For instance, the sheet resistance of NiSi layer is typically 1-5 Ohms/sq. and the sheet resistance of NiSi2 layer is 10-40 Ohms/sq. This translates to resistance increase of about 10 times after programming.

For conventional CoSi2 and TiSi2 fuse devices, the programming is based on silicide agglomeration. For NiSi fuse devices, the programming is based on phase change from NiSi to NiSi2. The energy used for phase change is much less than for agglomeration. As a result, the programming voltage of the NiSi fuse device is the much smaller as compared to conventional CoSi2 and TiSi2 fuse devices. The actual voltage depends on NiSi thickness and the sizes of the fuse structure. The low programming voltage makes this fuse device ideal for use in present IC process technologies that designed for low voltage applications.

Witness 1 initial: _____ Witness 2 initial: _____

The programming can be done without generating destructive damages in overlying dielectrics and underlying silicon layer. Thus the fuse structure does not have to be exposed to the air to be programmed as for some prior art fuse devices.

The size of the fuse structure can be the minimum width of the active region that design rules allow and can vary with different process technologies, STI space considerations, proximity effect, and other fuse design requirements. The number of contacts on fuse can vary although six contacts are shown in Fig.1. Multiple contacts in parallel may be used to reduce contact resistance and ensure that overheating will not occur within the contact vias.

Fig. 2 illustrates a side view of an example of the fusible connection device. The fuse device is disposed on poly Si on field oxide (SiO2) and is usually part of a larger integrated circuit device. The poly silicon layer could be undoped, P-type doped or N-type doped. In fact, the profile of the doping layer could be controlled so that it is totally consumed during the silicidation to keep the high resistance of silicon layer.

As shown in the figure, the proposed fuse device has additional advantage of being small and thus, inexpensive in silicon space. Furthermore, the process of this fuse device is compatible with conventional and does not require additional process steps. This will contribute to low cost for this fuse device.

This fuse device is not only good for bulk MOS technologies, but also suitable for other technologies especially SOI. In fact, in SOI as shown in Fig.3.

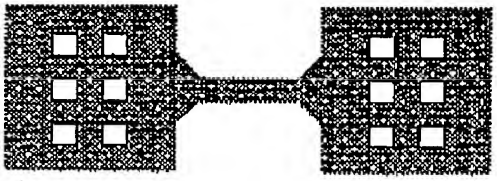

Fig.1. Top view of the proposed silicon silicide fuse device. The silicide layer is disposed on a silicon layer and programmed through contacts at each side.

Witness 1 initial: Witness 2 initial:

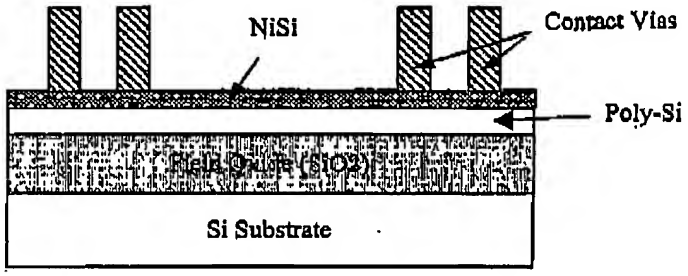

Fig. 2. A side view of the proposed silicon silicide fuse connection device for bulk technologies. The silicon layer can be doped, partial doped or undoped.

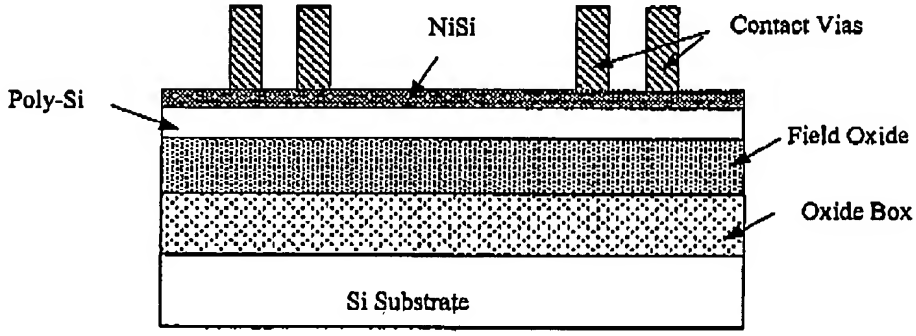

Fig. 3. A side view of the proposed NiSi fuse connection device on SOI. The poly-Si layer can be doped, partial doped or undoped.

Witness 1 initial: _____ Witness 2 initial: _____

AMD INVENTION DISCLOSURE Legal Dept ID#_____ Rec'd date _____
Sunnyvale x42110, return to MS 68, Texas x55964 return to MS 562

Advantages (check all that apply):

☐ avoids existing patent(s)	☐ improves precision	☐ simplifies manufacturing
☐ new function	☐ improves accuracy	☐ improves wear characteristic
☐ improves density	☐ improves efficiency	☐ improves signal to noise ratio
☐ increases operating speed	☐ fewer component parts	☐
☐ improves reliability	☐ reduces cost of manufacturing	☐

Discussion of advantage of the invention over other solutions
(*emphasize technical advance in the art* as measured against known art):

Date of first written description* of invention:	First external disclosure to (name):
Date of first drawing*: _____ Date invention first reduced to practice:	Date of first external disclosure, _____ none ☐ External disclosure under NDA* No ☐ Yes ☐
Made by (name): _____ Tested by (name):	First external disclosure or use by: presentation ☐, announcement ☐, sample ☐, sale ☐, offer for sale ☐
Date of first computer simulation:	Date of Non-Disclosure Agreement*, if any:
Date of first successful test:	Date of first publication*:
Country:	Publication name:
* *attach copy if possible*	Date of first commercial use:

Does plan exist to publish, disclose or sell? If so, where and when?_____

Invention was conceived, constructed or tested pursuant to the performance of a development contract with another company: No ☐ Yes ☐. If yes, Company name_____
Invention was jointly developed with participation of inventors from outside AMD. : No ☐ Yes ☐.
If yes, Company name_____

I have read and understood this disclosure and read and signed each page of the attachments:

Witness 1 signature: A.P. Marathe Date: 3/13/01
Printed name: AMIT P MARATHE Employee #: 24853

Witness 2 signature: A-l-l Date: 3/13/01
Printed name: MIKE LEE Employee #: 25593

After completing page 1, deliver to department reviewer. Patent Attorney date delivered

AMD INVENTION DISCLOSURE

Legal Dept. ID# [illegible] Rec'd date ____________
Sunnyvale x42110, return to MS 68, Texas x55964 return to MS 562

DISCLOSURE EVALUATION SECTION *(this page used by Reviewer)*

Does this invention add value to AMD's intellectual property portfolio? Yes ☐ No ☐
Explain: ____

Do you know of any related art? Yes ☐ No ☐ If yes, attach a copy and explain:

____

What application do you foresee for this invention? ____

____

I have reviewed this invention disclosure and it is ☐ is not ☐ recommended to AMD for patenting.
It should be: (A) given high ☐ normal ☐ low ☐ priority for patent application preparation,
(B) handled as a trade secret ☐, (C) published in order to block 2nd party patenting ☐, or
(D) further developed ☐.

Reviewer's signature: ____________________ Reviewer's printed name: ____________________
Employee #: __________ Date: ______________ *Patent Advocate signature required*

GUIDELINES AND CONSIDERATIONS FOR FOREIGN FILING DECISION

- *Identity of the locally-based competitors or potential competitors, and the users of locally based foundry service companies, in the country of interest.*
- *Existence of papers on topic of invention currently coming from this country (the inventor probably knows).*
- *Estimation of the effect on our business if this technology were put to use in this country by one or more of those companies.*
- *Likelihood of getting into a confrontation in this country over rights to this invention.*
- *Likelihood of a second party designing around this invention.*
- *Cost vs probable benefits: invention usage should be provable by inspection of product.*
- *The more fundamental and broadly applicable patents should receive more consideration regarding foreign filing than the more specific and therefor limited-in-scope patents.*

This invention is to be protected by filing patent applications in foreign countries checked below:

Japan ☐	S.Korea ☐	Taiwan ☐	UK ☐	France ☐	Germany ☐
Italy ☐	Netherlands ☐	Austria ☐	Switzerland ☐	Belgium ☐	Sweden ☐
NONE ☐	☐	☐	☐	☐	☐

Patent Attorney makes recommendation above. If foreign filing is checked route to [illegible] for signature

VP or Designate approves foreign filing (signature) ______________________________

AMD INVENTION DISCLOSURE

Legal Dept. Sunnyvale x42110, return to MS 68, Austin Texas x55964 return to MS 562

Rec'd date MAR 19 2001 AMD TECH. LAW DEPT.

AMD division / department:

Technology to which the invention applies: HIP7/HIP8...(Bulk/SOI...)

AMD product or process to which invention applies (if any): K7/K8.....

Working title of invention: NiSi Fuse Device

Inventor's signature : _____ **date :** _____
Inventor's printed full name: Qi Xinag Citizenship: China
Employee #: 24395 Extension: 44771 Mail stop: 143 Home telephone:(408)517-0879
Dept #: 7360 Division name: STG Supervisor: Ming-Ren Lin Director Dave Kyser VP: Craig Sander
Residence address: 1119 Thames Drive, San Jose, CA 95129
Post Office address: Same as above

Co-Inventor's signature : _____ date :_____
Co-Inventor's printed full name:_____ Citizenship:_____
Employee #:_____ Extension:_____ Mail stop:_____ Home telephone:( )_____
Dept #:_____Division name:_____Supervisor:_____ Director_____VP:_____
Residence address:_____
Post Office address:_____

Co-Inventor's signature : _____ date :_____
Co-Inventor's printed full name:_____ Citizenship:_____
Employee #:_____ Extension:_____ Mail stop:_____ Home telephone:( )_____
Dept #:_____Division name:_____Supervisor:_____ Director_____VP:_____
Residence address:_____
Post Office address:_____

List on additional sheet if there are more Co-Inventors and list total number of inventors here:_____

Name of requested Patent Application preparation Attorney , if known, _____

Witness 1 initial: QPM Witness 2 initial: ALL

AMD INVENTION DISCLOSURE Legal Dept ID#_____ Rec'd date _____
Sunnyvale x42110, return to MS 68, Texas x55964 return to MS 562

Identify known related art (patents, publications, products): Conventionally, people use EEPROM, Laser, oxide antifuse device and poly silicide (CoSi2/TiSi2) fuse device to form the discretionary connection function of a fuse device.

State the problem solved by this invention: This invention provide a small, nondestructive, process compatible and low voltage NiSi fuse device.

Brief description and/or sketch of invention (*please attach copies of AMD patent notebook pages, reports or drawings*):

In integrated circuits including CMOS ICs, it is often desirable to be able to permanently store information, or to form permanent connections on the circuits after it is manufactured. Fuse or devices forming fusible connection are frequently used for this purpose. Fuses can be used to program redundant elements to replace identical defective elements. Fuses can also be used to store die identification number or other information, or to adjust the speed of a circuit by adjusting the resistance of the signal path.

The conventional fuse devices, like EEPROM and oxide antifuse, need either thick oxide to sustain a charge on the floating node or much higher voltages than normal operating voltage supply, which are not viable for use on many of latest process technologies. Other conventional fuse devices, like the one is programmed using a laser to open link after the semiconductor device is processed and passivated, not only need extra processing step to blow and precise alignment to focus but also result in damages to the device and passivation layers.

This invention provides a small, nondestructive, process compatible and low voltage fuse device. As shown in Fig.1, a fusible link device is disposed on a semiconductor substrate. The fusible link device of the invention has a fresh non-programmed resistance and includes a nickel mono-silicide (NiSi) layer on top of silicon active layer. The NiSi layer is formed on the doped or undoped silicon layer. The electrical discontinuity is formed due to change of silicide phase from NiSi into high resistivity phase of nickel disilicide (NiSi2) when programming current is applied, such that the resistance of the fusible link device can be selectively increased to a higher programmed resistance. Because the NiSi layer has much lower sheet resistance than the NiSi2 layer, the resistance of the fuse device increases accordingly. For instance, the sheet resistance of NiSi layer is typically 1-5 Ohms/sq. and the sheet resistance of NiSi2 layer is 10-40 Ohms/sq. This translates to resistance increase of about 10 times after programming.

For conventional CoSi2 and TiSi2 fuse devices, the programming is based on silicide agglomeration. For NiSi fuse devices, the programming is based on phase change from NiSi to NiSi2. The energy used for phase change is much less than for agglomeration. As a result, the programming voltage of the NiSi fuse device is the much smaller as compared to conventional CoSi2 and TiSi2 fuse devices. The actual voltage depends on NiSi thickness and the sizes of the fuse structure. The low programming voltage makes this fuse device ideal for use in present IC process technologies that designed for low voltage applications.

The programming can be done without generating destructive damages in overlying dielectrics and underlying silicon layer. Thus the fuse structure does not have to be exposed to the air to be programmed as for some prior art fuse devices.

Witness 1 initial: Apm Witness 2 initial: A.L.L.

The size of the fuse structure can be the minimum width of the active region that design rules allow and can vary with different process technologies, STI space considerations, proximity effect, and other fuse design requirements. The number of contacts on fuse can vary although six contacts are shown in Fig.1. Multiple contacts in parallel may be used to reduce contact resistance and ensure that overheating will not occur within the contact vias.

Fig. 2 illustrates a side view of an example of the fusible connection device. The fuse device is disposed on silicon substrate and is usually part of a larger integrated circuit device. The silicon layer could be undoped, P-type doped or N-type doped. In fact, the profile of the doping layer could be controlled so that it is totally consumed during the silicidation to keep the high resistance of silicon layer.

As shown in the figure, the proposed fuse device has additional advantage of being small and thus, inexpensive in silicon space. Furthermore, the process of this fuse device is compatible with conventional and does not require additional process steps. This will contribute to low cost for this fuse device.

This fuse device is not only good for bulk MOS technologies, but also suitable for other technologies especially SOI. In fact, in SOI as shown in Fig.3.

Fig.1. Top view of the proposed silicon silicide fuse device. The silicide layer is disposed on a silicon layer and programmed through contacts at each side.

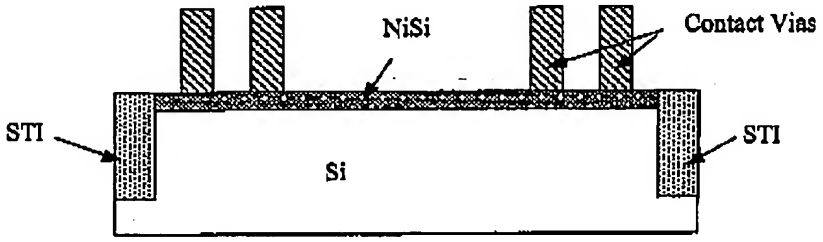

Fig. 2. A side view of the proposed silicon silicide fuse connection device for bulk technologies. The silicon layer can be doped, partial doped or undoped.

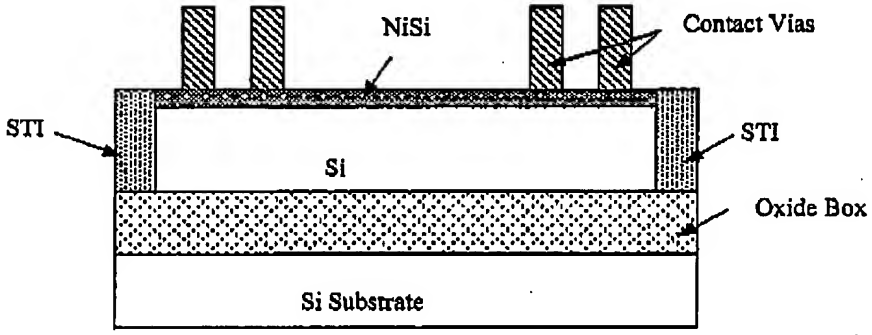

Fig. 3. A side view of the proposed NiSi fuse connection device on SOI. The silicon layer can be doped, partial doped or undoped.

Witness 1 initial: Alm Witness 2 initial: KLL

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AMD INVENTION DISCLOSURE Legal Dept ID# ________ Rec'd date ________
Sunnyvale x42110, return to MS 68, Texas x55964 return to MS 562

Advantages (check all that apply):

☐ avoids existing patent(s)	☐ improves precision	☐ simplifies manufacturing
☐ new function	☐ improves accuracy	☐ improves wear characteristic
☐ improves density	☐ improves efficiency	☐ improves signal to noise ratio
☐ increases operating speed	☐ fewer component parts	☐
☐ improves reliability	☐ reduces cost of manufacturing	☐

Discussion of advantage of the invention over other solutions
(*emphasize technical advance in the art* as measured against known art):

Date of first written description* of invention:	First external disclosure to (name):
Date of first drawing*: ________ Date invention first reduced to practice:	Date of first external disclosure, ________ none ☐ External disclosure under NDA* No ☐ Yes ☐
Made by (name): ________ Tested by (name):	First external disclosure or use by: presentation ☐, announcement ☐, sample ☐, sale ☐, offer for sale ☐
Date of first computer simulation:	Date of Non-Disclosure Agreement*, if any:
Date of first successful test:	Date of first publication*:
Country:	Publication name:
* *attach copy if possible*	Date of first commercial use:

Does plan exist to publish, disclose or sell? If so, where and when? ________

Invention was conceived, constructed or tested pursuant to the performance of a development contract with another company: No ☐ Yes ☐, If yes, Company name ________
Invention was jointly developed with participation of inventors from outside AMD. : No ☐ Yes ☐.
If yes, Company name ________

I have read and understood this disclosure and read and signed each page of the attachments:

Witness 1 signature: ________ Date: 3/13/01
Printed name: AMIT P. MARATHE Employee #: 24853

Witness 2 signature: ________ Date: 3/13/01
Printed name: MIKE LEE Employee #: 25593.

[illegible]

AMD INVENTION DISCLOSURE Legal Reg'd# _____ Rec'd date _____
Sunnyvale x42110, return to MS 68. Texas x55964 return to MS 562

DISCLOSURE EVALUATION SECTION (*this page used by Reviewer*)

Does this invention add value to AMD's intellectual property portfolio? Yes ☐ No ☐
Explain: _____

Do you know of any related art? Yes ☐ No ☐ If yes, attach a copy and explain:

What application do you foresee for this invention? _____

I have reviewed this invention disclosure and it **is** ☐ **is not** ☐ recommended to AMD for patenting.
It should be: (A) given **high** ☐ **normal** ☐ **low** ☐ priority for patent application preparation,
(B) handled as a **trade secret** ☐, (C) **published** in order to block 2nd party patenting ☐, or
(D) **further developed** ☐.

Reviewer's signature: _____ Reviewer's printed name: _____
Employee #: _____ Date: _____ *Patent Advocate signature required*

GUIDELINES AND CONSIDERATIONS FOR FOREIGN FILING DECISION

- *Identity of the locally-based competitors or potential competitors, and the users of locally based foundry service companies, in the country of interest.*
- *Existence of papers on topic of invention currently coming from this country (the inventor probably knows).*
- *Estimation of the effect on our business if this technology were put to use in this country by one or more of those companies.*
- *Likelihood of getting into a confrontation in this country over rights to this invention.*
- *Likelihood of a second party designing around this invention.*
- *Cost vs probable benefits: invention usage should be provable by inspection of product.*
- *The more fundamental and broadly applicable patents should receive more consideration regarding foreign filing than the more specific and therefor limited-in-scope patents.*

This invention is to be protected by filing patent applications in foreign countries checked below:

Japan ☐	S.Korea ☐	Taiwan ☐	UK ☐	France ☐	Germany ☐
Italy ☐	Netherlands ☐	Austria ☐	Switzerland ☐	Belgium ☐	Sweden ☐
NONE ☐	☐	☐	☐	☐	☐

Patent Advocate make recommendation above if foreign filing is checked, send to DVP for signature

VP or Designate approves foreign filing (signature) _____